Fig. 1
Prior art

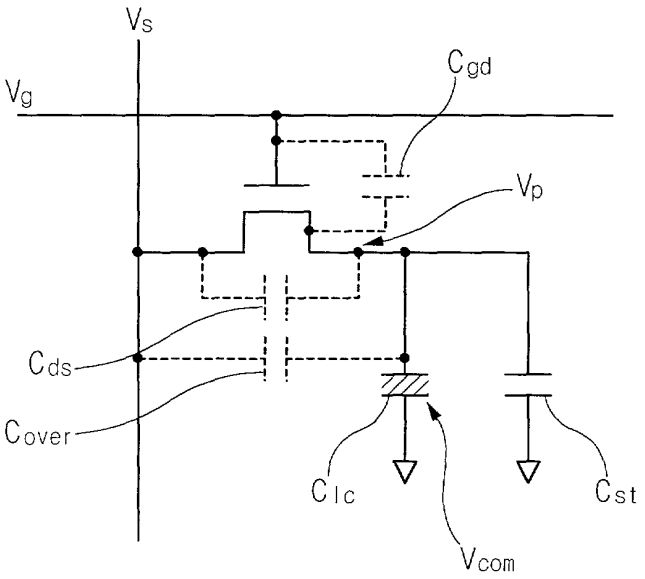


Fig. 2
Prior art

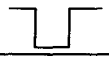
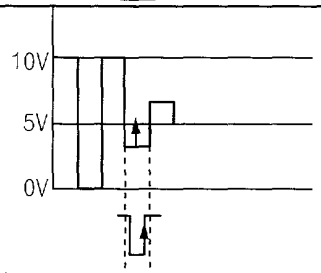
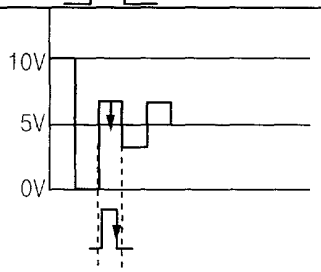
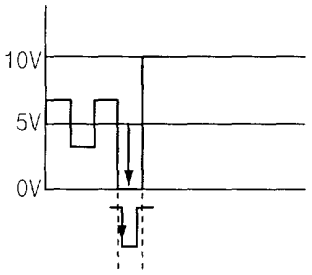
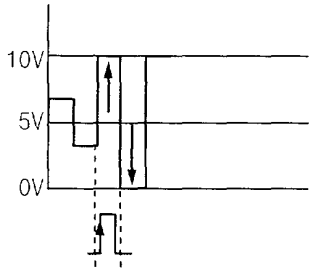
	(+)→(-) Inversion	(-)→(+) Inversion
Form of Pulse signal application to storage COM		
□Dielectric constnat - High → Low □Voltage - High → Low □Gray - High → Low	 Effect of approximating data signal to COM signal	 Effect of approximating data signal to COM signal
□Dielectric constnat - Low → High □Dielectric constnat - Low → High □Dielectric constnat - High → Low	 Overshoot of data voltage	 Overshoot of data voltage

Fig. 3
Prior art

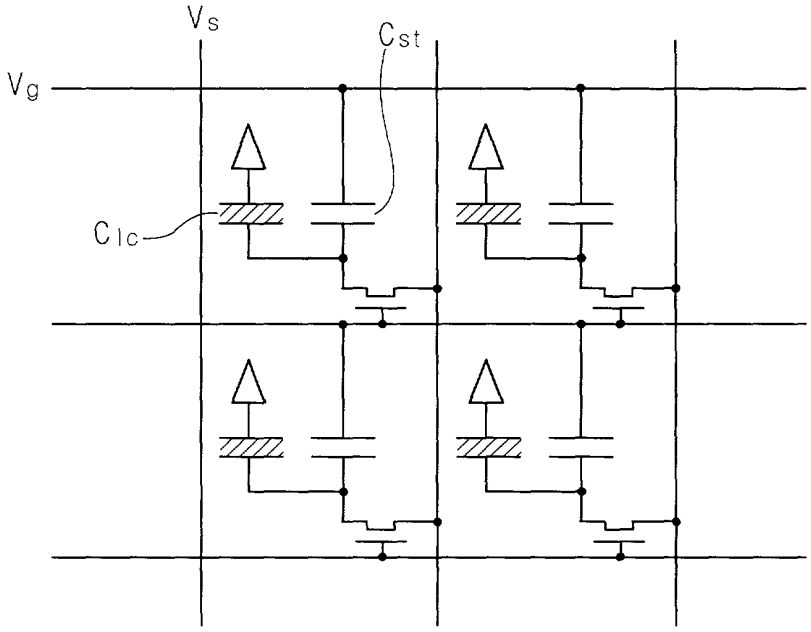


Fig. 4
Prior art

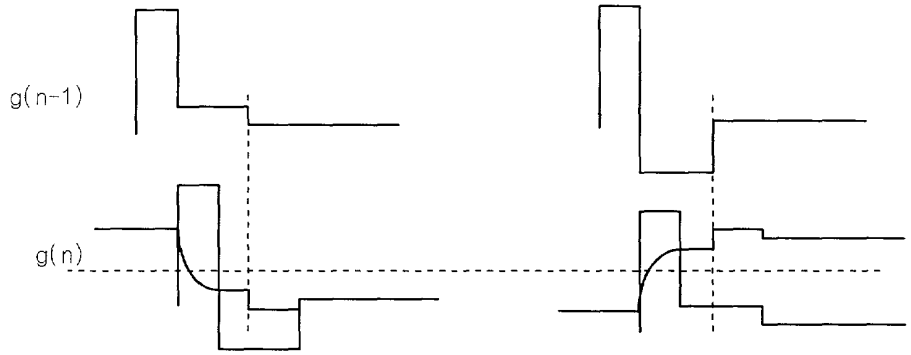


Fig. 5

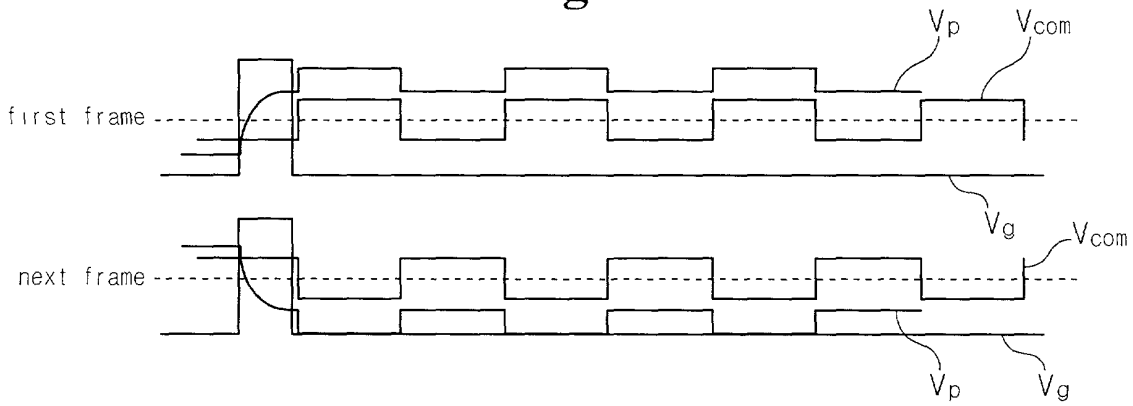


Fig. 6

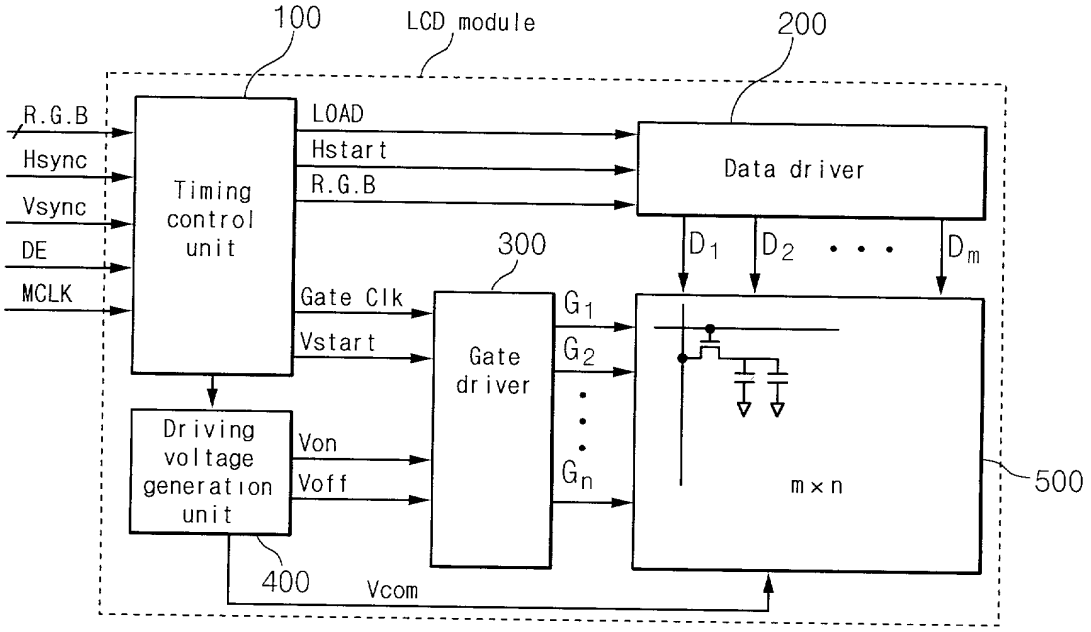

100
LCD module
200
R.G.B
Hsync
Vsync
DE
MCLK
Timing control unit
LOAD
Hstart
R.G.B
Data driver
D1
D2
Dm
300
Gate Clk
Vstart
Gate driver
G1
G2
Gn
Driving voltage generation unit
Von
Voff
m×n
500
400
Vcom

Fig. 7

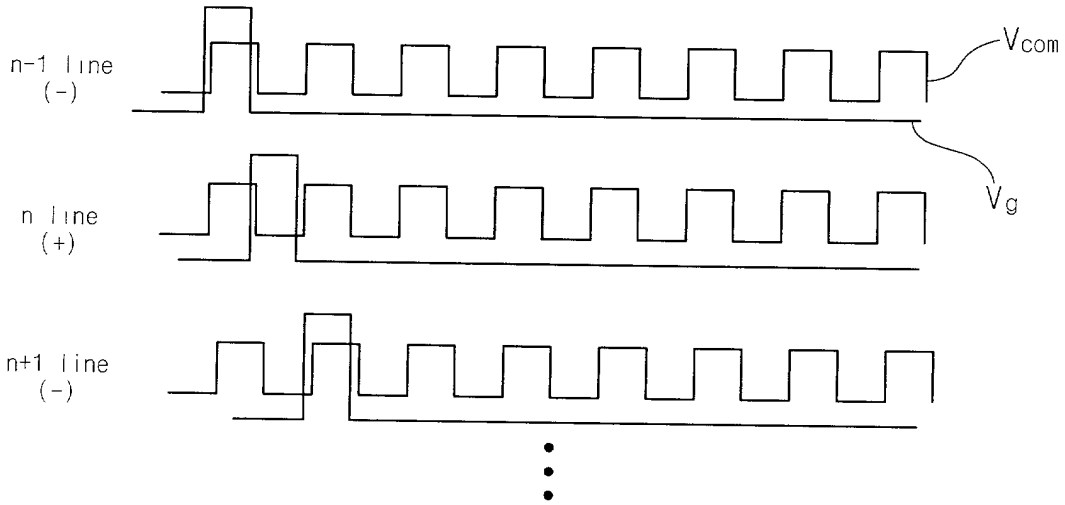

n-1 line
(-)
Vcom
Vg
n line
(+)
n+1 line
(-)

Fig. 8

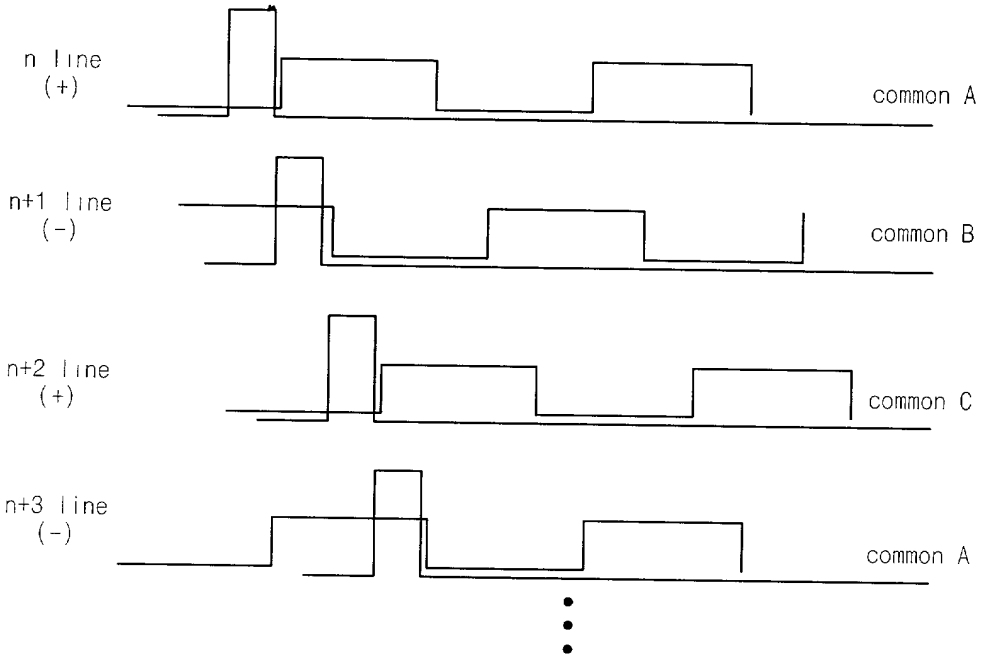


Fig. 9

Prior art

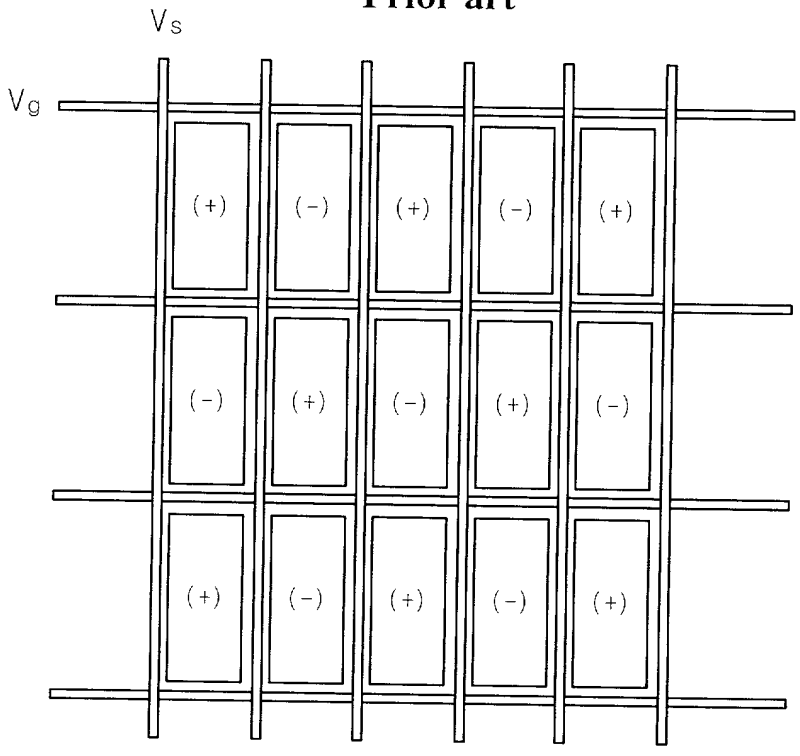


Fig. 10

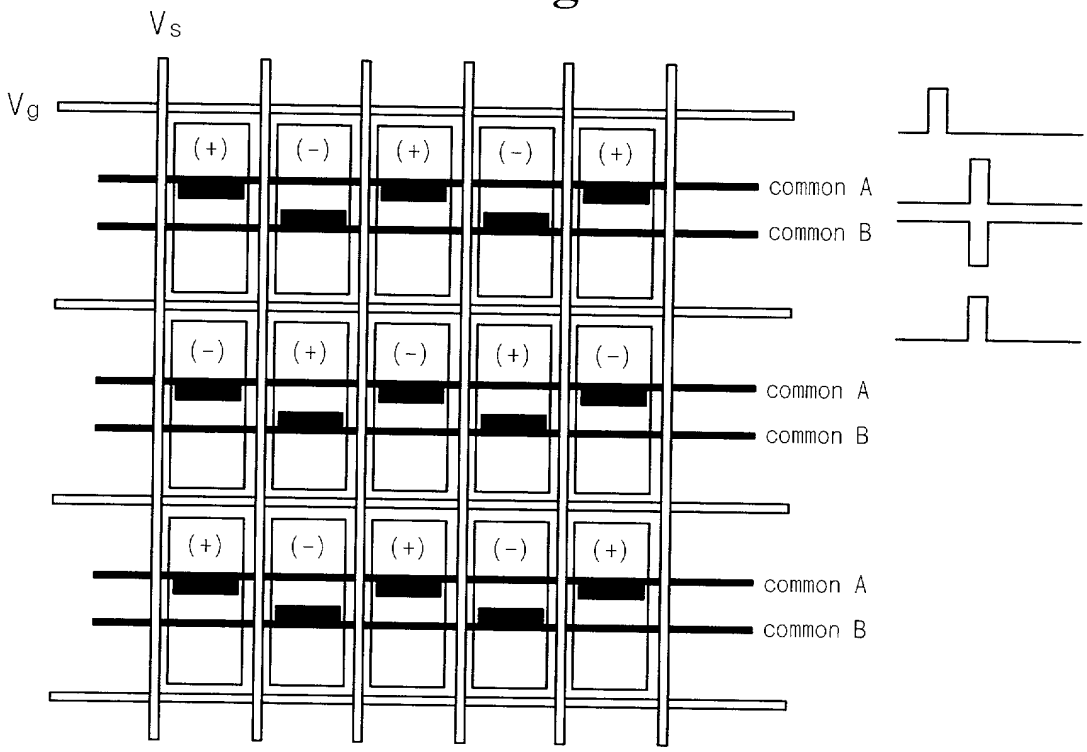

Vs
Vg
(+)
(-)
common A
common B

Fig. 11

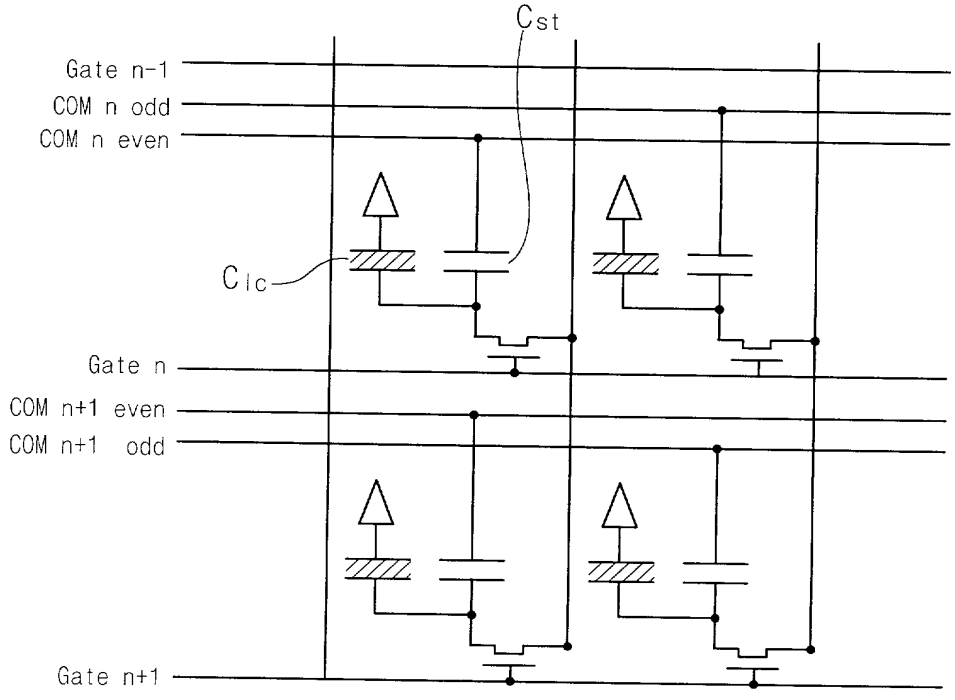

Cst
Gate n-1
COM n odd
COM n even
Clc
Gate n
COM n+1 even
COM n+1 odd
Gate n+1

Fig. 12

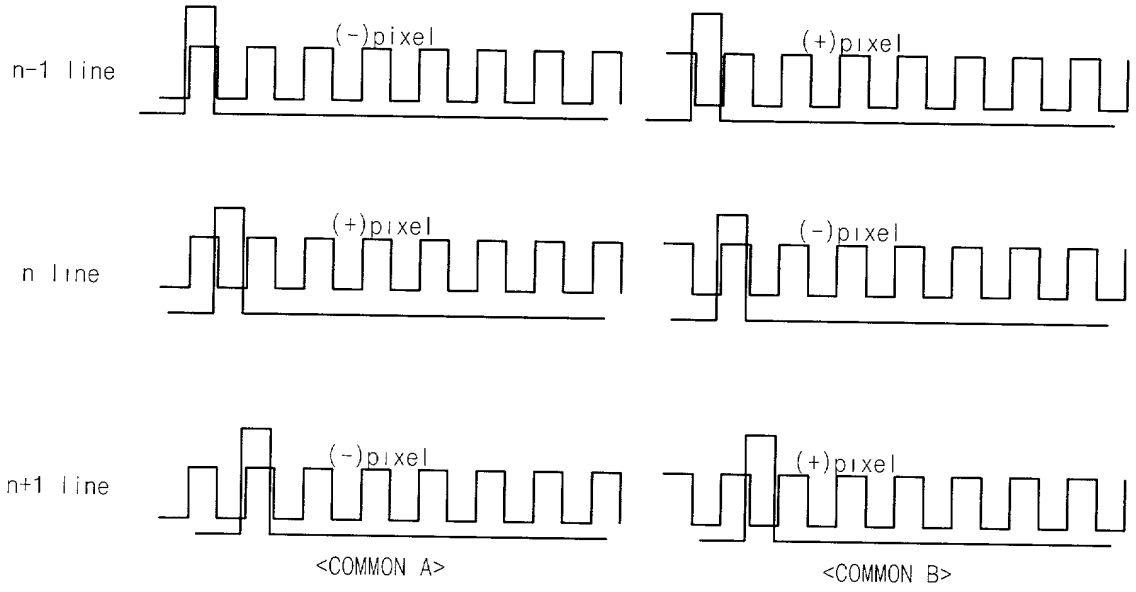

n-1 line
(-)pixel
(+)pixel
n line
(+)pixel
(-)pixel
n+1 line
(-)pixel
(+)pixel
<COMMON A>
<COMMON B>

Fig. 13

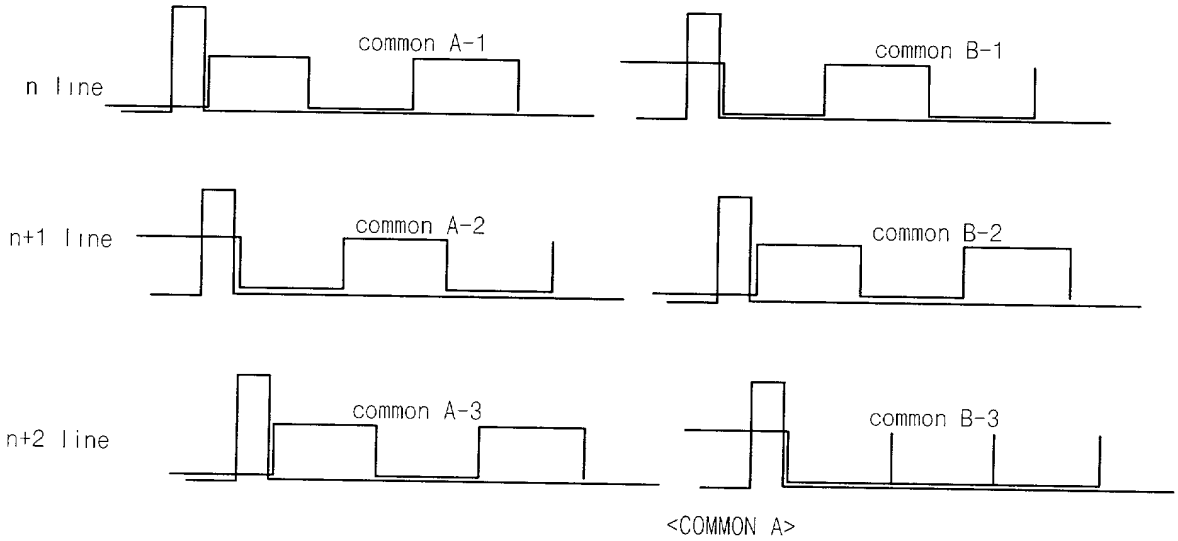

n line
common A-1
common B-1
n+1 line
common A-2
common B-2
n+2 line
common A-3
common B-3
<COMMON A>

Fig. 14

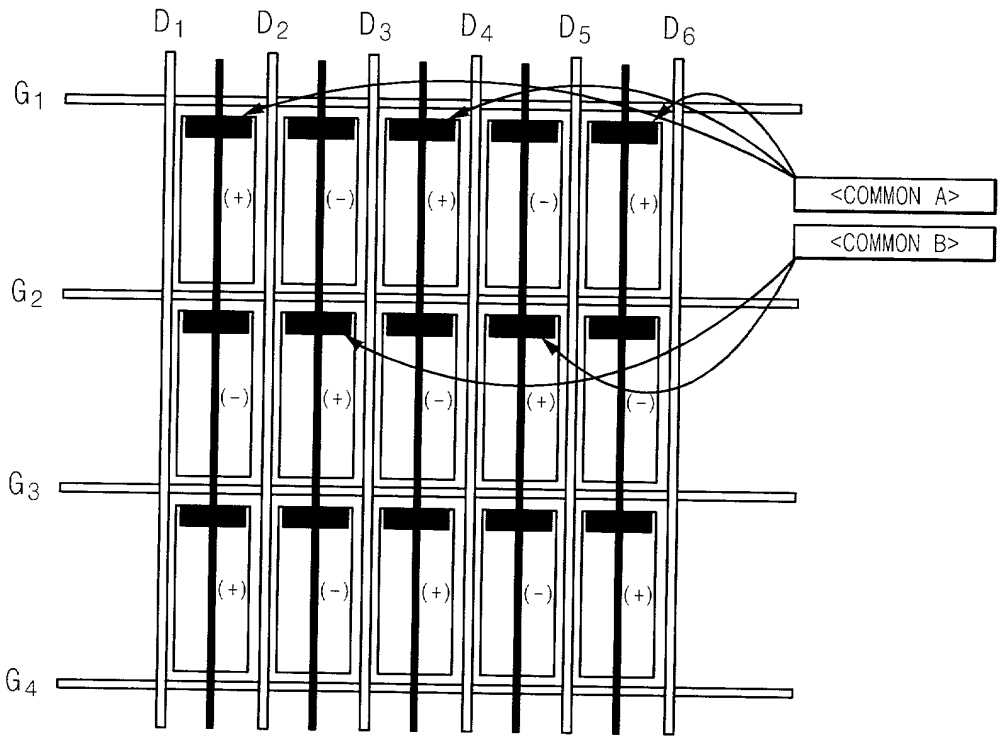


Fig. 15

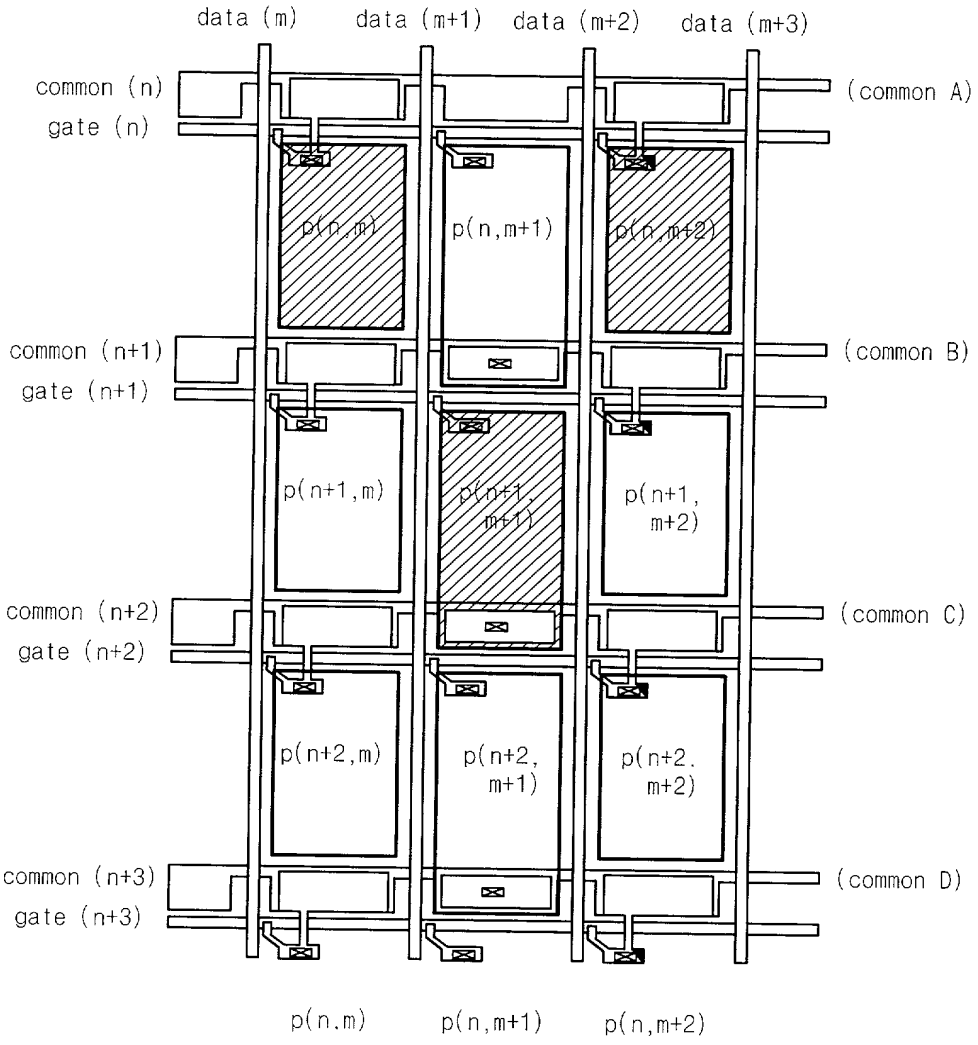

data (m)
data (m+1)
data (m+2)
data (m+3)
common (n)
gate (n)
(common A)
p(n,m)
p(n,m+1)
p(n,m+2)
common (n+1)
gate (n+1)
(common B)
p(n+1,m)
p(n+1, m+1)
p(n+1, m+2)
common (n+2)
gate (n+2)
(common C)
p(n+2,m)
p(n+2, m+1)
p(n+2, m+2)
common (n+3)
gate (n+3)
(common D)
p(n,m)
p(n,m+1)
p(n,m+2)

Fig. 16

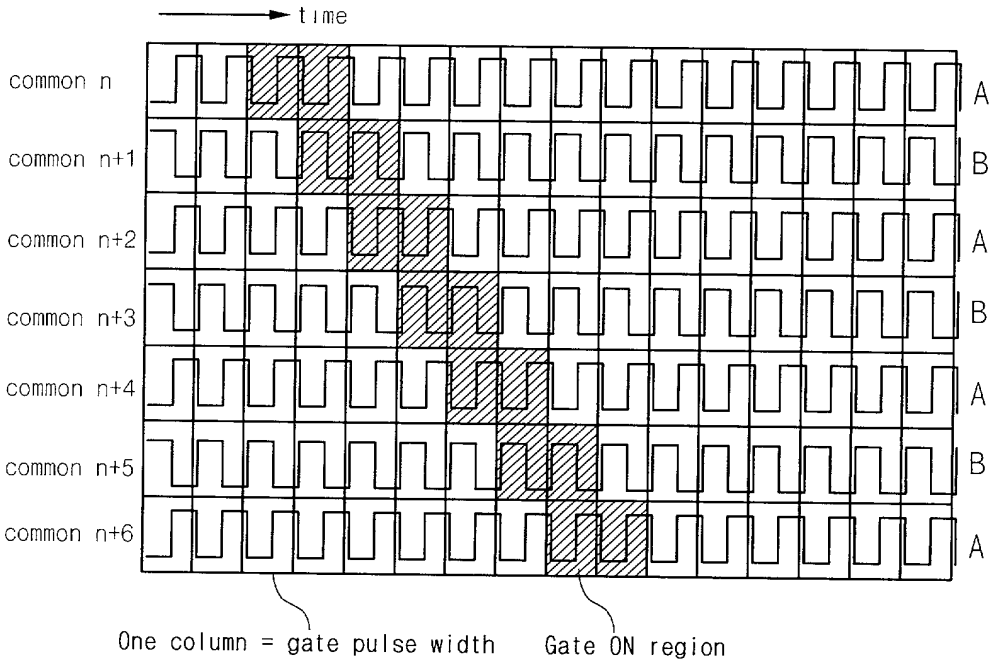

time
common n
common n+1
common n+2
common n+3
common n+4
common n+5
common n+6
A
B
A
B
A
B
A
One column = gate pulse width
Gate ON region

Fig. 17

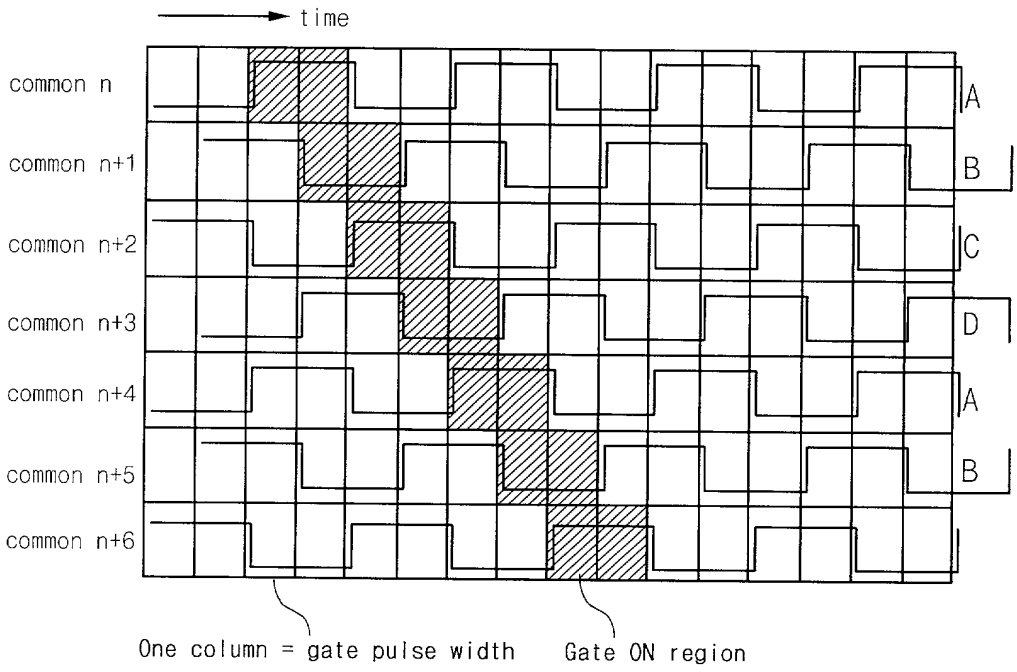

time
common n
common n+1
common n+2
common n+3
common n+4
common n+5
common n+6
A
B
C
D
A
B
One column = gate pulse width
Gate ON region

Fig. 18

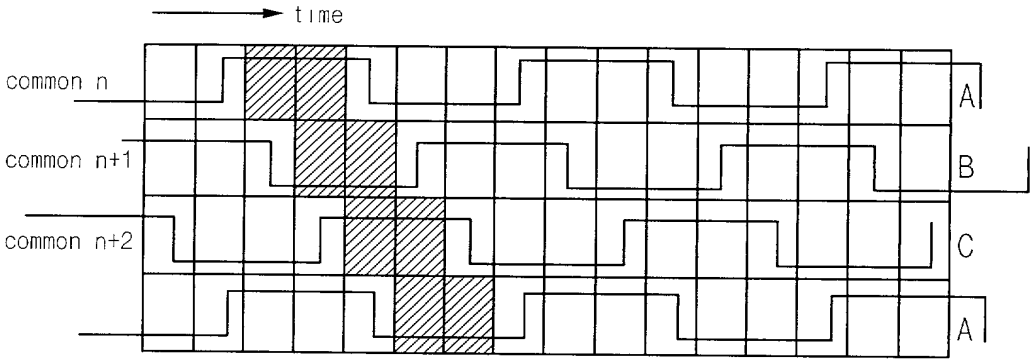

time
common n
common n+1
common n+2
A
B
C
A

Fig. 19

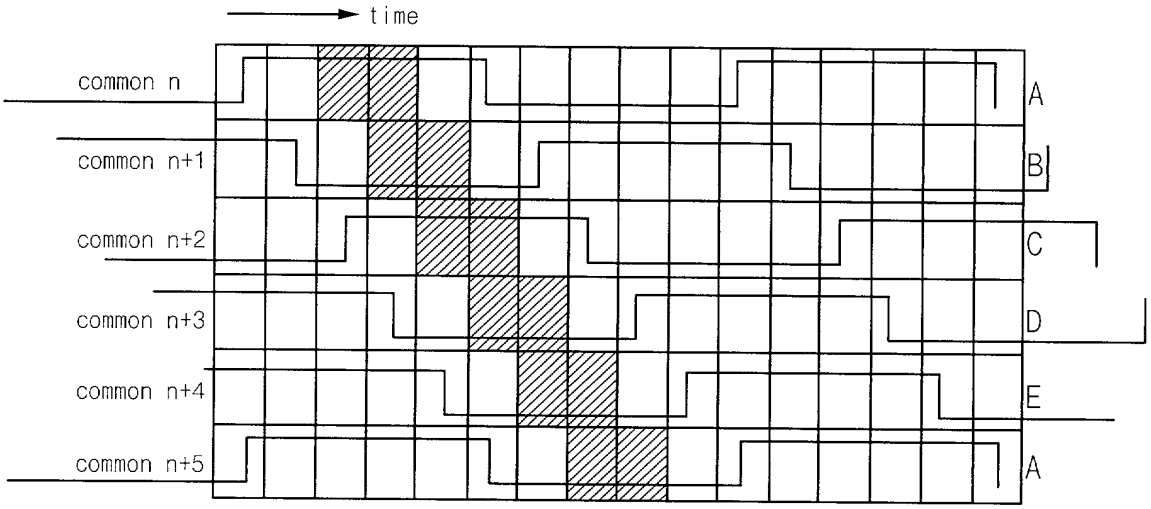
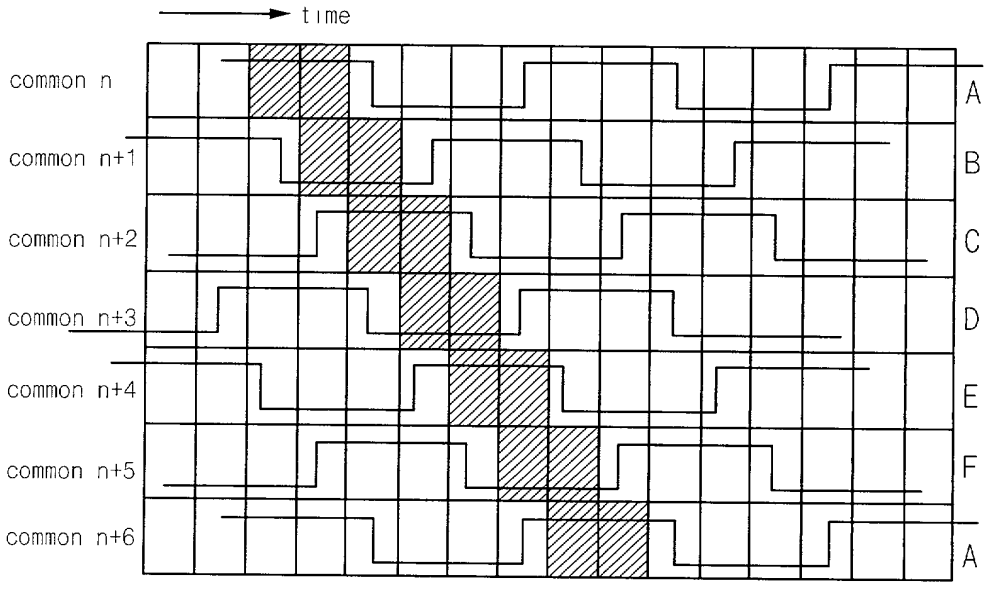

time
common n
common n+1
common n+2
common n+3
common n+4
common n+5
A
B
C
D
E
A

Fig. 20


time
common n
common n+1
common n+2
common n+3
common n+4
common n+5
common n+6
A
B
C
D
E
F
A

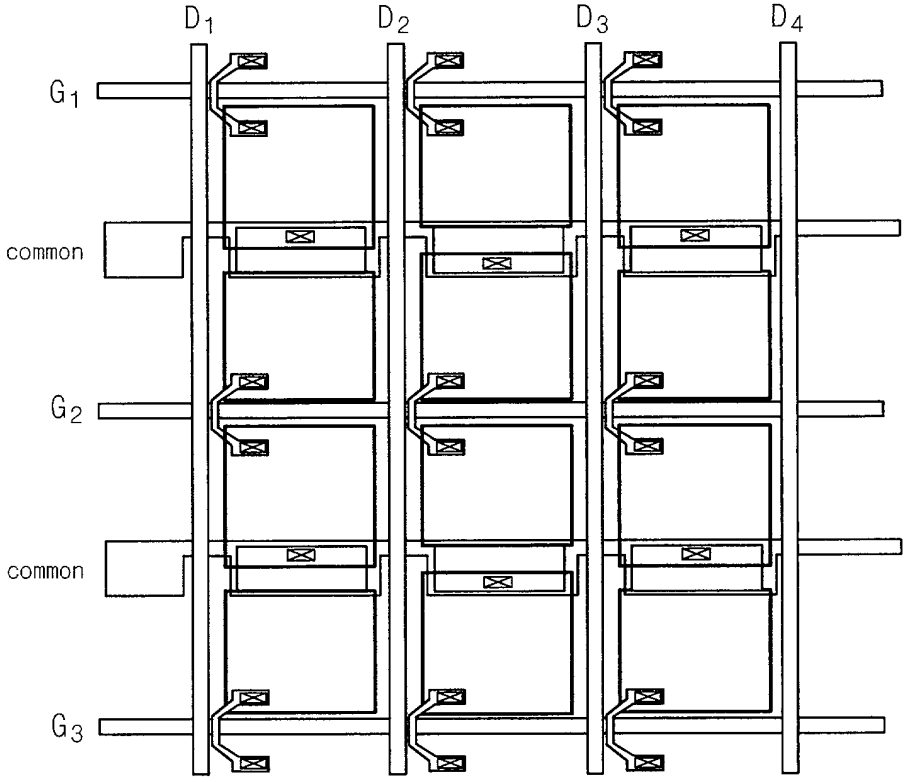



Fig. 21